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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,009	12/19/2001	Hong Sung Song	049128-5055	8778

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EXAMINER	
BODDIE, WILLIAM	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 05/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/021,009	SONG, HONG SUNG	
	Examiner	Art Unit	
	William Boddie	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/19/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. To enter a new IDS the Applicant reopened prosecution, filing a Request for Continued Examination on 10/19/05. Upon updating of the searches new pertinent prior art was discovered by the Examiner. As such the applicable rejections have been applied below. Claims 1-13 are currently pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 5,648,793).

With respect to claim 1, Chen discloses, a method of driving a liquid crystal display panel of a dot inversion system (fig. 4(c); col. 3, lines 63-65) having liquid crystal cells (p11-p44 in fig. 1a) arranged at intersections between a plurality of data lines (D1-D4 in fig. 1a) and a plurality of gate lines (G1-G4 in fig. 1a) in a matrix array, comprising the steps of:

supplying the data lines with (n-2)th data (D1 value at T3 in fig. 5) corresponding to the liquid crystal cells connected to an (m-2)th gate line (G1 in fig. 5), wherein m and n are integers both greater than or equal to 2;

conducting a first data supplying channel (note the selection pulse on G# at T# in fig. 5) for the liquid crystal cells connected to the mth gate line (G3 in fig. 5) such that the (n-2)th data is supplied to the liquid crystal cells connected to the mth gate line; and

conducting a second data supplying channel for the liquid crystal cells connected to the (m-2)th gate line (G1 in fig. 5) such that the (n-2)th data is supplied to the liquid crystal cells connected to the (m-2)th gate line (note the voltage of pixel P11 in fig. 5),

wherein conducting the first data supplying channel and conducting the second data supplying channel are performed simultaneously (both G1 and G3 are driven simultaneously at T3 in fig. 5; col. 3, lines 45-47).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Asada et al. (US 5,867,141).

With respect to claim 2, Chen discloses, the method according to claim 1 (see above).

Chen discloses precharging the first and second gate lines at every frame with data signals (T1, T2 in fig. 5; col. 3, lines 39-45).

Chen does not expressly disclose that the first and second gate lines are precharged during a blanking interval.

Asada discloses precharging a first and second gate line with data signals applied during a blanking interval (abstract and col. 5, lines 18-38).

Chen and Asada are analogous art because they are both from the same field of endeavor namely, gate driving methods of liquid crystal displays.

At the time of the invention it would have been obvious to one of ordinary skill in the art to drive the LCD of Chen during T1-T2 as a blanking interval.

The motivation for doing so would have been to generate images with competent image quality and a stable high contrast (Asada; col. 3, lines 64-65).

Therefore it would have been obvious to combine Asada with Chen for the benefit of image quality and contrast to obtain the invention as specified in claim 2.

With respect to claim 3, Chen and Asada disclose, the method according to claim 2 (see above).

Chen further discloses, wherein polarity inversion of the data signals (D1 in fig. 5) applied to the liquid crystal cells connected to the first and second gate lines (G1, G2 in fig. 5) is made in at least two clock time intervals prior to an application of an active data signal (T3 for G1 and T4 for G2) (the pre-charge data must undergo polarity inversion prior to be applied (prior to T1 for G1), this is clearly two clock intervals prior to the application of active data (T3 for G1); also note col. 3, lines 39-45 and col. 4, lines 26-31).

With respect to claim 4, Chen and Asada disclose, the method according to claim 2 (see above).

Chen further discloses, wherein gate and data control signals for applying data to the liquid crystal cells connected to the first and second gate lines (G1 and G2 in fig. 5) are applied in at least two clock time intervals before the gate and data control signals become effective data (fig. 5; Chen delays the control signals applied to the first and second gate lines; and also discloses different lengths of driving pulses; col. 3, lines 42-45; col. 4, lines 26-31).

6. Claims 5, 10 and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Miyahara et al. (US 6,075,507).

With respect to claim 5, Chen discloses, a driving apparatus for a liquid crystal display panel of a dot inversion system (fig. 4(c); col. 3, lines 63-65) having liquid crystal cells (p11-p44 in fig. 1a) arranged at intersections between a plurality of data lines (D1-D4 in fig. 1a) and a plurality of gate lines (G1-G4 in fig. 1a) in a matrix array comprising:

continuously generating first and second gate start pulses such that data corresponding to an (n-2)th data line is supplied to an nth data line, wherein n is an integer greater than or equal to 2 (fig. 5; col. 3, lines 45-47).

Chen does not expressly disclose, a data/gate driving integrated circuit or a pre-charging controller.

Miyahara discloses, a data driving integrated circuit supplying data to the data lines of the liquid crystal display panel (2 in fig. 4);

a gate driving integrated circuit responding to a gate start pulse to sequentially drive the gate lines of the liquid crystal display panel (3 in fig. 4, col. 6, lines 7-10); and

a timing generator circuit (5 in fig. 4).

Chen and Miyahara are analogous art because they are both from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

At the time of the invention it would have been obvious to one of ordinary skill in the art to include the driving apparatus', taught by Miyahara, in the LCD panel of Chen.

The motivation for doing so would have been the familiarity with which these devices are associated with in the art, thereby decreasing the complexity of the circuitry involved.

Therefore it would have been obvious to combine Miyahara with Chen for the benefit of familiarity to obtain the invention as specified in claim 5.

With respect to claim 10, currently it appears that claim 10 is merely a broader version of claim 5, as it is exempt from the limitations of sequential gate driving and use of the dot inversion system. Therefore claim 10 is rejected based on the same merits shown above in the rejection of claim 5.

With respect to claims 12-13, as these claims are identical limitations to claims 3 and 4, claims 12-13 are rejected on the same merits shown above in claims 3 and 4.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Miyahara et al. (US 6,075,507) and further in view of Iino et al. (US 5,900,856).

With respect to claim 6, Chen and Miyahara disclose, the apparatus according to claim 5 (see above).

Neither Chen nor Miyahara expressly disclose the inner circuitry of the pre-charging controller.

Iino discloses, a pre-charging controller (fig. 40) includes:

a first input line supplied with a pre-gate start pulse (LP in fig. 40) and a second input line supplied with a data enable signal (E in fig. 40) for controlling data output of the data driving integrated circuit (col. 39, lines 32-34);

first delay means for delaying the pre-gate start pulse from the first input lien by one clock interval of the data enable signal (253s in fig. 40);

second delay means for delaying the delayed pre-gate start pulse from the first delay means by one clock interval of the data enable signal (253t in fig. 40); and

a gate device (253-5 in fig. 40) for executing an exclusive logical sum operation of the pre-gate start pulse from the first input line and an output signal of the second delay mean to continuously output the first and second gate start pulses (col. 40, line 66 – col. 41, lines 7).

Iino, Chen and Miyahara are all analogous art because they are from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

At the time of the invention it would have been obvious to replace the gate driver timing controller of Chen and Miyahara with a pre-charging controller taught by Iino.

The motivation for doing so would have been to minimize power consumption (Iino; col. 40, lines 20-22).

Therefore it would have been obvious to combine Iino with Chen and Miyahara for the benefit of lessened power consumption to obtain the invention as specified in claim 6.

8. Claims 7-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5,648,793) in view of Miyahara et al. (US 6,075,507) and further in view of Asada et al. (US 5,867,141).

With respect to claim 7, Chen and Miyahara disclose, the apparatus according to claim 5 (see above).

Also shown above Asada discloses a blanking interval (see rejection of claim 2).

Asada, Miyahara and Chen are all analogous art because they are from the same field of endeavor namely, LCD panel gate driving methods and circuitry.

For further motivation and means of combining see the above rejection of claim 2.

With respect to claim 8-9, Chen, Miyahara and Asada disclose, the apparatus according to claim 7 (see above).

As claims 8-9 are identical limitations to those recited in claims 3-4 they are rejected on the same merits shown above.

With respect to claims 11, as claim 11 recites identical limitations as claim 7, claim 11 is rejected on the same merits shown above in the rejection of claim 7.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Will Boddie whose telephone number is (571) 272-0666. The examiner can normally be reached on Monday through Friday, 7:30 - 4:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Wlb
5/2/06

AMR A. AWAD
PRIMARY EXAMINER